A PHASE-LOCKED LOOP CIRCUIT WITH CURRENT-PULSE INJECTION FOR IMPROVING LINEARITY

PRIORITY CLAIM

[1] This application claims priority from Italian patent application No. MI2003A000484, filed March 14, 2003, which is incorporated herein by reference.

TECHNICAL BACKGROUND

[2] An embodiment of the present invention relates generally to a Phase-Locked Loop (PLL) circuit.

BACKGROUND

[3] A PLL is a fundamental component of many electronic systems (for example, in telecommunication applications). The PLL consists of a negative feedback circuit that allows multiplication of the frequency of a reference signal by a selected conversion factor; this results in the generation of a tuneable and stable output signal with the desired frequency.

[4] For this purpose, a frequency divider scales the frequency of the output signal by the conversion factor. The resulting signal is fed back to a phase comparator, which detects a phase difference between the feedback signal and the reference signal; the phase comparator outputs a control current indicative of the phase difference. A loop-filter integrates the control current into a corresponding voltage, which controls the frequency of the output signal accordingly. In a lock condition, the frequency of the feedback signal matches the frequency of the reference signal; therefore, the frequency of the output signal will be equal to the reference frequency multiplied by the conversion factor.

[5] A problem that adversely affects operation of the PLL is the non-linearity of the phase comparator. Typically, the phase comparator is implemented with a charge pump that is controlled by a Phase Frequency Detector (PFD). The PFD consists of two flip-flops, which are set in response to the raising edge of the reference signal and of the feedback signal, respectively; the two flip-flops are reset when both the reference signal and the feedback signal are asserted. The charge pump includes two current generators consisting of a high-side PMOS and a low-side NMOS; the PMOS is controlled by the value latched in the flip-flop

associated with the reference signal, whereas the NMOS is controlled by the value latched in the flip-flop associated with the feedback signal.

[6] The phase comparator has an input/output characteristic (plotting an output charge against an input phase difference) that significantly differs from an ideal straight line. A typical non-linearity is caused by the mismatch between the PMOS and the NMOS in the charge pump. A further non-linearity is introduced by the asymmetrical variation of non-linear capacitances in the PFD. An additional source of non-linearity consists of the dead zone of the charge pump. The non-linearity in the I/O characteristic of the phase comparator is generally higher when the phase difference takes values near to zero (because of the different behaviour of the PMOS and of the NMOS in the charge pump).

[7] The above-mentioned problem is particularly acute in a PLL of the fractional type; in this case, the dividing ratio of the frequency divider changes dynamically so as to obtain an average conversion factor equal to a fractional number. However, the change in the dividing ratio causes fractional spurious signals (or spurs) at frequency offsets from a carrier that are multiples of the periodicity in the division pattern. The non-linearity of the phase comparator strongly increases the level of the fractional spurs, with a negative impact on the performance of the whole PLL.

[8] Several solutions have been proposed in the last years for reducing the effects of the above-mentioned non-linearity of the phase comparator.

[9] A typical configuration of the phase comparator addresses the problem caused by the dead zone of the charge pump by introducing a delay line on the path of the signal used to reset the flip-flops in the PFD.

[10] Moreover, some implementations force the phase comparator to work in a linear part of its I/O characteristic; this result is achieved keeping the phase difference between the feedback signal and the reference signal different from zero in the lock condition. For example, a solution known in the art consists of generating two separate reset signals for the flip-flops in the PFD by means of asymmetric delay lines. A different solution is based on the injection of a direct current into the loop filter. In both cases, the PLL locks when the total current provided to the loop filter in every cycle is zero. In this condition, the reference

signal and the feedback signal have the same frequency, but a pre-defined phase difference.

[11] However, the solutions described above strongly increase the level of reference spurs at an offset around the carrier that is equal to the reference frequency. This problem is caused by the fact that, although zero on the average, the current injected into the loop filter has an instantaneous value that is different from zero. As a consequence, the control voltage output by the loop filter exhibits a ripple at the operative frequency of the phase comparator.

SUMMARY

[12] Briefly, an embodiment of the present invention provides a phase-locked loop circuit for providing an output signal having a frequency depending on the frequency of a reference signal, the circuit including means for deriving a feedback signal from the output signal, means for providing a control signal indicative of a phase difference between the reference signal and the feedback signal, means for controlling the frequency of the output signal according to the control signal, and means for causing the circuit to enter a lock condition when the reference signal and the feedback signal have the same frequency and a pre-defined phase difference, wherein the means for causing the circuit to enter the lock condition includes means for conditioning the control signal to have an instantaneous value substantially zero in the lock condition by means of a conditioning signal consisting of a series of pulses each one corresponding to the pre-defined phase difference.

[13] Moreover, a corresponding synthesising method is also encompassed in an embodiment of the invention.

DESCRIPTION OF DRAWINGS

[14] Further features and the advantages of the solution according to the present invention will be made clear by the following description of a preferred embodiment thereof, given purely by way of a non-restrictive indication, with reference to the attached figures, in which:

FIG. 1 shows the functional blocks of a PLL implementing the solution of an embodiment of the invention,

FIG. 2a is a schematic block diagram of a phase comparator of the PLL of **FIG. 1** according to an embodiment of the invention,

FIGS. 2b and 2c are simplified time diagrams describing operation (in a lock condition) of a PLL according to the prior art and to an embodiment of the present invention, respectively,

FIG. 3a depicts a preferred implementation of a conditioning circuit of the PLL of **FIG. 1** in combination with its frequency divider according to an embodiment of the invention, and

FIG. 3b describes operation of the conditioning circuit of **FIG. 3a** in a simplified time diagram according to an embodiment of the invention.

DETAILED DESCRIPTION

[15] With reference in particular to **FIG. 1**, a digital PLL **100** of the fractional type is shown. The PLL ***100*** is used to synthesise an output signal ***Vo*** with a desired frequency Fo (defining a channel of operation of the PLL ***100***). The output signal ***Vo*** is obtained by multiplying a frequency Fr of a reference signal ***Vr*** by a selected conversion factor; the reference signal ***Vr*** is generated by a quartz oscillator (not shown in the figure), which provides a stable and accurate time base.

[16] The PLL ***100*** implements a feedback loop through a frequency divider ***105*** that receives the output signal ***Vo***. The frequency divider ***105*** is controlled by two external signals N and K. The parameter N defines an integer component of the selected channel. The parameter K is an adjusting value K consisting of an integer varying from 0 to a modulus F (with the value K/F that defines a fractional component of the channel). The block ***105*** divides the frequency Fo of the output signal ***Vo*** alternatively by N or N+1, according to the adjusting value K. The resulting signal ***Vb*** (having a frequency Fb) is fed back to a phase comparator ***115***.

[17] The block ***115*** compares the feedback signal ***Vb*** with the reference signal ***Vr***. The phase comparator ***115*** outputs a control current ***Id*** indicative of the phase difference between the two signals, which current ***Id*** is injected into a loop filter ***120***. The loop filter ***120*** removes the high frequency components of the control current ***Id***; moreover, it integrates the control current ***Id*** into a

corresponding voltage ***Vc***. The control voltage ***Vc*** drives a Voltage-Controlled Oscillator (VCO) ***125***, which provides the output signal ***Vo***.

[18] During operation of the PLL ***100***, the VCO ***125*** starts oscillating at a free-run frequency as a consequence of background noise in the circuit. Assuming that the adjusting value K is equal to 0, the above-described system operates as a PLL of the integer type. In this case, the frequency divider 105 always divides the frequency Fo of the output signal ***Vo*** by N, so that Fd=Fo/N.

[19] In an unlock condition (such as during an initial power up or immediately after a channel switching), the frequency Fb of the feedback signal ***Vb*** is different from the frequency Fr of the reference signal ***Vr***. Therefore, the phase comparator ***115*** outputs a corresponding control current ***Id***. The resulting control voltage ***Vc*** (from the loop filter ***120***) changes the frequency Fo of the output signal ***Vo*** accordingly. Particularly, when the feedback frequency Fb is lower than the reference frequency Fr, the control voltage ***Vc*** instructs the VCO ***125*** to increase the output frequency Fo; conversely, when the feedback frequency Fb is higher than the reference frequency Fr, the control voltage ***Vc*** instructs the VCO ***125*** to reduce the output frequency Fo.

[20] After a transient period, the frequency Fb of the feedback signal ***Vb*** reaches the frequency Fr of the reference signal ***Vr*** (with ***Vc***=0). In this lock condition, the frequency Fo of the output signal ***Vo*** is thus equal to Fr*N. Therefore, the PLL **100** delivers an output signal ***Vo*** with a frequency Fo having any desired value that is a multiple of the frequency Fr of the reference signal ***Vr*** (according to N); in other words, the output frequency Fo can be adjusted (across a band of interest) with a resolution, or channel spacing, equal to the reference frequency Fr.

[21] An unavoidable consequence of the above-described process is that the frequency multiplication performed by the PLL ***100*** raises the contribution to a phase noise of the output signal ***Vo*** (due to the frequency divider ***105***) according to a quadratic law of the value N; therefore, N must be kept relatively low, with consequent high channel spacing. Moreover, the phase comparator ***115*** generates transient noise at its operative frequency Fr (because of spikes due to the finite speed of its circuit components); this interference can be represented as

(reference) spurs at offsets of +/-Fr around a carrier Fo. The reference spurs are filtered by the loop filter ***120***. Unfortunately, the bandwidth of the loop filter ***120*** cannot be too narrow since that would increase the phase noise and a settling time required to switch between different channels. Again, the frequency Fr of the reference signal ***Vr*** must be kept relatively high.

[22] The above-mentioned drawbacks of the integer PLLs are solved by a fractional architecture, wherein the dividing ratio of the frequency divider ***105*** changes dynamically in the lock condition. Particularly, in F cycles, K times the frequency Fo of the output signal ***Vo*** is divided by N+1 rather than by N. The average dividing ratio over F cycles is then:

$$\frac{K(N+1)+(F-K)N}{F} = N + \frac{K}{F}$$

As a consequence, in the lock condition the frequency Fo of the output signal ***Vo*** is equal to (N+K/F)Fr.

[23] The fractional architecture allows frequency resolution that is a fractional portion of the reference frequency Fr; therefore, the reference frequency Fr can be higher than the channel spacing (with a consequent reduction of the value N). In this way, the performance of the PLL 100 in term of both the phase noise and the settling time is improved. For example, a channel spacing of 30KHz can be achieved (with F=16) using a reference frequency Fr=16*30kHz=480kHz; for a PLL working in a band of 900MHz, the value N=Fo/Fr is then 900MHz/480KHz=1875 (instead of 900MHz/30kHz=30.000 for a corresponding integer architecture).

[24] However, the changes in the frequency division carried out by the block ***105*** cause additional spurs, with a periodicity equal to 1/(K*F/Fr). These (fractional) spurs are at offsets multiple of +/-Fr/F around the carrier Fo. The fractional spurs are generally of greater magnitude than the reference spurs, and reside on the adjacent channels in the worst settings defined by the fractional channels 1/F and (F-1)/F. Therefore, the fractional spurs cannot be removed by the loop filter ***120***; in fact, that would require a too-narrow loop bandwidth (with an intolerable increase of the phase noise and of the settling time in the PLL ***100***).

[25] However, the concepts of the present invention are also applicable when the PLL has a different structure or includes equivalent elements, when the PLL works with different reference frequency, channel spacing and/or operative parameters, and the like.

[26] Moving now to **FIG. 2a**, the phase comparator ***115*** includes a Phase Frequency Detector (PFD) **205**; the PFD **205** detects a phase difference between the feedback signal ***Vb*** and the reference signal ***Vr*** either lower than +/-2π radians or higher than +/-2π radians (commonly referred to as frequency difference).

[27] For this purpose, the reference signal ***Vr*** is applied to the clock terminal of a D-type flip-flop **210r**; the (input) D-terminal of the flip-flop ***210r*** is connected to the positive terminal of a direct-voltage power supply +Vdd (for example, 5V with respect to a reference voltage or ground). Likewise, the feedback signal ***Vb*** is applied to the clock terminal of a further D-type flip-flop ***210b***; the D-terminal of the flip-flop ***210b*** is connected to the power supply terminal.

[28] The (output) Q-terminal of the flip-flop ***201r*** and the Q-terminal of the flip-flop ***201b*** are connected to respective input terminals of an AND-gate ***215***. The signal output by the AND-gate ***215*** is supplied, through a delay line ***220***, to the reset terminals of both the flip-flop ***210r*** and the flip-flop ***210b***.

[29] The (inverted) Q-terminal of the flip-flop ***210r*** provides a phase-indicator up-signal Su; the signal Su is underlined to denote that it is at a low logic value (0) when asserted and at a high logic value (1) when deasserted. The Q-terminal of the flip-flop ***210d*** directly provides a phase-indicator down-signal Sd.

[30] The signals Su and Sd control a charge pump (CP) ***225***. The charge pump ***225*** includes a high-side leg (referred to the power supply voltage +Vdd) and a low-side leg (referred to ground). The high-side leg consists of a current generator ***230h*** (providing a current ***Ih***), which is connected in series to an electronic switch ***232h*** (typically implemented with a PMOS); likewise, the low-side leg consists of a current generator ***230l*** (providing a current ***Il***), which is connected in series to an electronic switch ***232l*** (typically implemented with an NMOS). The switch **232h** and the switch ***232l*** are controlled by the up-signal Su and by the down-signal Sd, respectively. The high-side leg and the low-side leg

are connected to each other, and define an output terminal of the charge pump 225 that supplies a current ***Ip***.

[31] As described in detail in the following, a conditioning circuit **235** provides a signal Sc. The conditioning signal Sc controls an electronic switch ***240*** (for example, implemented with a PMOS). A further current generator 242 is connected between the switch ***240*** and the output terminal of the charge pump ***225***; the generator ***242*** sinks a conditioning current ***Ic*** from the output terminal of the charge pump ***225***. The resulting control current ***Id=Ip-Ic*** is then provided to the loop filter.

[32] Considering **FIGS. 2a** and **2b** together, the up-signal Su is asserted upon detection of a raising edge of the reference signal ***Vr***; in response thereto, the switch ***232h*** is closed and the current ***Ih*** is injected into the output terminal of the charge pump ***225***. Likewise, the down-signal Sd is asserted upon detection of a raising edge of the feedback signal ***Vb***; the switch ***232l*** is then closed and the current ***Il*** is sunk from the output terminal of the charge pump ***225***. When both signals Su and Sd are asserted, the flip-flops **210b** and ***210r*** are reset; as a consequence, the switches ***232h***, ***232l*** are opened so as to zero the corresponding currents ***Ih***,***Il***. The delay line ***220*** ensures that the flip-flops ***210r***, ***210b*** are reset with a short delay removing the effects of the dead zone of the charge pump ***225***.

[33] The charge-pump current ***Ip*** then consists of a series of pulses indicative of the phase difference between the signals ***Vb*** and ***Vr***. Particularly, each pulse of the charge-pump current ***Ip*** has a width proportional to the magnitude of the phase difference; the pulse is positive when the raising edge of the feedback signal ***Vb*** follows the raising edge of the reference signal ***Vr***, or it is negative otherwise.

[34] In a PLL known in the art (see **FIG. 2b**), the conditioning current ***Ic*** consists of a direct current that is provided to the loop filter. The PLL locks when the total control current ***Id=Ip-Ic*** injected into the loop filter in every cycle is zero (*i.e.*, the positive area is the same as the negative area). In this condition shown in the figure, the feedback signal ***Vb*** and the reference signal ***Vr*** have the same frequency, but a phase difference corresponding to the value of the conditioning

current ***Ic***. However, the instantaneous value of the control current ***Id*** is different from zero; this causes a ripple (at the reference frequency Fr) in the control voltage ***Vc*** provided to the VCO, with a corresponding increase in the level of the reference spurs.

[35] Conversely, as shown in **FIG. 2c**, in the solution according to an embodiment of the present invention the conditioning current ***Ic*** consists of a series of pulses. Preferably, the pulses of the conditioning current ***Ic*** are synchronous with the feedback signal ***Vb***; particularly, a leading edge of each pulse of the conditioning current ***Ic*** is generated in response to a corresponding raising edge of the feedback signal ***Vb***. The pulse has a predefined width (for example, 1-2ns).

[36] The PLL locks when the pulses of the charge-pump current ***Ip*** match the pulses of the conditioning current ***Ic***; in this condition shown in the figure, the control current ***Id*** has an instantaneous value that is always zero. As a consequence, the frequency Fb of the feedback signal ***Vb*** is the same as the frequency Fr of the reference signal ***Vr***. However, the feedback signal ***Vb*** and the reference signal ***Vr*** have a phase difference corresponding to the width of the pulses of the conditioning current ***Ic*** (with the raising edges of the feedback signal ***Vb*** that follow the corresponding raising edges of the reference signal ***Vr***).

[37] However, the concepts of the present invention are also applicable when the PFD is replaced with a mixer or XOR-gates, or when the charge pump has another structure (for example, reversing the positions of the current generators and of the switches in every leg); similar considerations apply if the transistors PMOS and NMOS are replaced with equivalent components, if the conditioning current is injected into the output terminal of the charge-pump (by means of a current generator controlled by a PMOS), and the like. Alternatively, the up signal and the down signal are generated in response to the leading edges of the reference signal and of the feedback signal, respectively, or the PFD provides equivalent signals indicative of the phase difference between the feedback signal and the reference signal.

[38] An implementation of the conditioning circuit ***235*** (based on the signals available in the frequency divider ***105***) is shown in **FIG. 3a**. Particularly, the

frequency divider ***105*** includes a dual-modulus divider **305**. The block ***305*** divides the frequency Fo of the output signal ***Vo*** by either P or P+1 (wherein P is a predefined integer); in this way, a simple continuous division mechanism can be achieved controlling the number of times to divide by P or P+1. For example, a 3/4 divider allows accomplishing a ratio of 608/202=3.01 by dividing the frequency Fo of the output signal ***Vo*** by 3 a total of 200 times and by 4 twice (608=3*200+4*2 and 202=200+2).

[39] Operation of the dual-modulus divider **305** is controlled by a logic ***310*** according to the value N and the adjusting value K. The result of the frequency division performed by the dual-modulus divider ***305*** consists of a pre-scaled signal ***Vs*** (having a frequency Fs), which is used to clock the other elements of the frequency divider ***105*** and for resetting the control logic ***310***; the same pre-scaled signal ***Vs*** is also used to clock the conditioning circuit **235**. A counter ***315*** (for example, with modulus 16) generates the feedback signal ***Vb*** dividing the frequency Fs of the pre-scaled signal ***Vs*** by its modulus (i.e., Fb=Fs/16).

[40] The conditioning circuit ***235*** includes a decoder ***320***, which receives the content of the counter ***315***. The decoder ***320*** outputs a signal S_6, which is applied to the D-terminal of a flip-flop ***325*** (clocked by the pre-scaled signal ***Vs***). The Q-terminal of the flip-flop ***325*** directly provides the conditioning signal Sc.

[41] Considering **FIGS. 3a** and **3b** together, the feedback signal ***Vb*** is kept low for 8 periods of the pre-scaled signal ***Vs*** (each one consisting of 3 periods of the output signal ***Vo***) and goes high for the next 8 periods thereof (each one consisting of 3 or 4 periods of the output signal ***Vo***); particularly, the raising edge of the feedback signal ***Vb*** is generated when the counter **315** reaches the value 8. The decoder ***320*** asserts the signal S_6 when the counter ***315*** takes the value 6 (*i.e.*, in response to the raising edge of the pre-scaled signal ***Vs*** preceding the one causing the raising edge of the feedback signal ***Vb*** by 2 periods).

[42] The signal S_6 exhibits a skew, with respect to the pre-scaled signal ***Vs***, due to the delay introduced by the decoder ***320***. The signal S_6 is latched by the flip-flop ***325*** in response to the next raising edge of the pre-scaled signal ***Vs***. As a consequence, the conditioning signal Sc (provided by the Q-terminal of the flip-flop ***325***) remains asserted for one period of the pre-scaled signal ***Vs*** (from the

value 7 to the value 8 of the counter ***315***). In this way, the leading edge of each pulse of the conditioning signal Sc is synchronous with a corresponding raising edge of the feedback signal ***Vb***. Moreover, the pulse has a well-defined width; in the example at issue, the pulse of the conditioning signal Sc lasts one period of the pre-scaled signal ***Vs***, that is 3 periods of the output signal ***Vo***.

[43] However, the concepts of an embodiment of the present invention are also applicable when the frequency divider has a different structure, or when the conditioning circuit includes equivalent components. Similar considerations apply if another multi-modulus divider is provided, if the counter has a different modulus, or if the conditioning signal is synchronized with the feedback signal in another way. Alternatively, each pulse of the conditioning signal has a different width, or the conditioning circuit allows programming this width to any desired number of periods of the output signal.

[44] More generally, an embodiment of the present invention proposes a phase-locked loop circuit, which is used for providing an output signal having a frequency depending on the frequency of a reference signal. The circuit includes means for deriving a feedback signal from the output signal. Further means are used for providing a control signal, which is indicative of a phase difference between the reference signal and the feedback signal. The frequency of the output signal is controlled according to the control signal. Moreover, means are provided for causing the circuit to enter a lock condition when the reference signal and the feedback signal have the same frequency and a pre-defined phase difference. In the solution of the invention, the means for causing the circuit to enter the lock condition includes means for conditioning the control signal to have an instantaneous value substantially zero in the lock condition; this result is achieved by means of a conditioning signal, which consists of a series of pulses each one corresponding to the pre-defined phase difference.

[45] The solution of an embodiment of the invention strongly reduces the effects of the non-linearity in the input/output characteristic of the phase comparator included in the PLL.

[46] The proposed structure forces the phase comparator to work in a linear part of its I/O characteristic; this result is achieved conditioning the control current

(or any other equivalent signal) to have an instantaneous value that is always zero in the lock condition.

[47] The conditioning schema of an embodiment of the invention does not affect the level of the reference spurs (as in the solutions known in the art).

[48] Therefore, an embodiment of the devised solution results in an improvement of the overall performance of the PLL.

[49] The preferred embodiment of the invention described above offers further advantages.

[50] Particularly, the conditioning current is added to the charge-pump current.

[51] Therefore, the resulting current injected into the loop filter can be conditioned (to be always zero in the lock condition) in a very simple manner.

[52] A typical application of the proposed solution is in a PLL including a PFD, which provides an up signal and a down signal that are asserted in response to corresponding comparison edges of the reference signal and of the feedback signal, respectively.

[53] This structure is well suited for the generation of the pulses of the conditioning current.

[54] Advantageously, the pulses of the conditioning current are generated synchronously with a selected one between the reference signal and the feedback signal.

[55] The proposed feature makes it possible to obtain the conditioning current with few simple components.

[56] However, the solution according to an embodiment of the present invention lends itself to be implemented in a PLL having a different architecture, injecting the conditioning current in another position, or even generating the conditioning current in a different way.

[57] In a preferred embodiment of the invention, the conditioning current is derived from the signal output by the PLL.

[58] An embodiment of the devised solution provides a very high accuracy (since it is based on the most accurate high-frequency time base source available in the circuit).

[59] As a further enhancement, the leading edges of the conditioning current correspond to the raising edges of the feedback signal.

[60] This choice reduces the noise introduced by the frequency divider (since the effects of any spike caused by the switching of the feedback signal have disappeared at the next comparison).

[61] A way to further improve the solution is to clock the conditioning circuit by means of the pre-scaled signal generated in the frequency divider.

[62] The proposed structure makes it possible to exploit components that are already available in the PLL.

[63] Alternatively, the conditioning signal can be generated using an inverting delay line driven by the reference signal or the feedback signal; this embodiment is very simple, but introduces a jitter in the output signal due to the width variance in the pulses of the conditioning signal (which variance is proportional to the width itself). Moreover, an embodiment of the present invention is also suitable to be implemented generating the raising edges of the conditioning signal in response to the raising edges of the feedback signal, clocking the conditioning circuit in another way (for example, by means of a dedicated circuit), or even with a different structure of the conditioning circuit.

[64] Without detracting from general applicability, an embodiment of the devised solution is particularly advantageous in a PLL of the fractional type.

[65] In fact, the proposed conditioning schema is very effective in the reduction of the fractional spurs (without increasing the level of the reference spurs).

[66] However, the implementation of an embodiment of the invention in a PLL of the integer type is not excluded (even if the linearity is not usually critical in this case). Moreover, the same conditioning schema can be used also in a PLL without any frequency divider, which PLL always outputs a signal having the same frequency as the reference signal.

[67] The circuit ***100*** may be part of an electronic system, such as, for example, a computer system or wireless communication device.

[68] Naturally, in order to satisfy local and specific requirements, a person skilled in the art may apply to the solution described above many modifications and alterations all of which, however, are included within the scope of protection of embodiments the invention.